Raster Address (RA0-RA4)

RA0-RA4 are row-address signals which are used to select the row of the current character in the font cell memory to be displayed.

Cursor Display (CUDISP)

CUDISP is an active high-level video signal which is used to display the cursor on the CRT screen at the current display location. This output is inhibited while DISPTMG is low. This output is mixed with the video signal and is provided to the CRT display circuits.

Light Pen Strobe (LPSTB)

LPSTB is an active high-level input signal which accepts a strobe pulse detected by the light pen and control circuit. When this signal is activated, the memory address (MA0-MA11), along with the current settings of HIRES and DOTADR, are stored in the 14bit light-pen register. The stored memory address needs to be corrected in software, taking the delay time of the display device, light pen, and light-pen-control circuits into account.

INTERNAL REGISTERS

ADDRESS REGISTER (AR)

AR is a 5-bit register used to select among the 18 internal control registers (R0-R17). The value of AR is the address of one of 18 internal control registers. Data values from 18 to 31 do nothing. Access to R0-R17 requires writing the address of the corresponding control register into this register.

HORIZONTAL TOTAL REGISTER (R0)

The contents of R0 program the total number of horizontal character-clock periods per line, including the retrace period. The data is 8-bit, and its value should be programmed according to the selected mode of the display. The programmed value must be one less than the number of character intervals required. When programming for interlace mode, the value must be even.

HORIZONTAL DISPLAYED REGISTER (R1)

R1 is used to program the number of displayed characters per horizontal line. Data is 8-bit, and any value smaller than that in R0 is valid.

HORIZONTAL SYNC POSITION REGISTER (R2)

The contents of R2 program the horizontal sync position in units of the character-clock period. Data is 8-bit, and any value less than R0 is valid. The value programmed should be one less than the sync position desired. The effect of increasing the value in R2 is to shift all characters displayed on the CRT screen to the left. When the value is decreased, character positions shift to the right.

SYNC WIDTH REGISTER (R3)

The contents of R3 set the horizontal sync pulse width and the vertical sync pulse width. The horizontal sync pulse width is programmed in the lower 4 bits, in units of the character-clock period (0 is invalid). The vertical sync pulse width is programmed in the upper 4 bits, in units of the horizontal period. When 0 is programmed in the upper 4 bits, 16 horizontal periods are specified.

VERTICAL TOTAL REGISTER (R4)

R4 is used to program the total number of horizontal scans per frame, including the vertical retrace period. This is a 7-bit value and should be programmed according to the selected display mode. The programmed value should be one less than the number desired.

VERTICAL TOTAL ADJUST REGISTER (R5)

The contents of R5 select the total number of horizontal scans per field. This register allows fine control of the deflection frequency.

VERTICAL DISPLAYED REGISTER (R6)

R6 is used to determine the number of displayed character rows on the CRT screen. This is a 7-bit value, and any number that is smaller than that in R5 is valid.

Table D-2: Pulse Width of Vertical Sync Signal

VSW				PULSE WIDTH
2^7	2^6	2^5	2^4	(# Rows)
0	0	0	0	16H
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

NOTE: H=horizontal period.

Table D-3: Pulse Width of Horizontal Sync Signal

HSW				PULSE WIDTH
2^3	2^2	2^1	2^0	(# Characters)
0	0	0	0	(not used)
0	0	0	1	1CH
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

NOTE: CH=character period; HSW=0 cannot be used.

VERTICAL SYNC POSITION REGISTER (R7)

The contents of R7 set the vertical sync position on the screen, in units of the horizontal character line period. Data is 7-bit, and any number that is equal to or less than the vertical total register can be programmed. The value programmed should be one less than the position desired. Increasing the value shifts the display upward. Decreasing the values shifts the display downward.

INTERLACE AND SKEW REGISTER (R8)

R8 programs the raster-scan mode and the skew (delay) of CUDISP and DISPTMG.

INTERLACE MODE PROGRAM BITS (V, S)

The raster-scan mode is selected by the V and S bits.

Table D-4: Interlace Mode (D0, D1)

V BIT	S BIT	RASTER-SCAN MODE
0	0	Noninterlace mode
1	0	Noninterlace mode
0	1	Interlace sync mode
1	1	Interlace sync and video mode

SKEW PROGRAM BIT (C1, C0, D1, D0)

The C1, C0, D1, and D0 bits are used to program the skew (delay) of CUDISP and DISPTMG.

The skews of the two signals are programmed separately.

Table D-5: DISPTMG Skew Bit (D7, D6)

D1 BIT	D0 BIT	DISPTMG SIGNAL
0	0	Zero skew
0	1	One-character skew
1	0	Two-character skew
1	1	No output

Table D-6: Cursor Skew Bit (D5, D4)

C1 BIT	C0 BIT	NON SKEW
0	0	Zero skew
0	1	One-character skew
1	0	Two-character skew
1	1	No output

The skew function is used to delay the CUDISP and DISPTMG signals for optimum screen-memory access, dot-matrix memory, and video signal timing.

MAXIMUM RASTER ADDRESS REGISTER (R9)

R9 is used to program the maximum raster address (5 bits). This register defines the number of rasters (lines) per character, including intercharacter spaces. Programming is as follows:

▶ Noninterlace Mode

In the following tabulation, the value parameter is set at 4.

RASTER ADDRESS	RESULTING FORMAT
0	- - - - - - - - - -
1	- - - - - - - - - -
2	- - - - - - - - - -
3	- - - - - - - - - -
4	- - - - - - - - - -

NOTE: The number of rasters produced in the character format is 5 (one more than the value programmed).

▶ Interlace Sync Mode

In the following tabulation, the value parameter is 4.

RASTER ADDRESS	RESULTING FORMAT
0	- - - - - - -
0	. . . . .
1	- - - - - - -
1	. . . . .
2	- - - - - - -
2	. . . . .
3	- - - - - - -
3	. . . . .
4	- - - - - - -
4	. . . . .

NOTE: - - - - - - - and . . . . . denote alternate fields.

The total number of rasters in the character is 10. The number is found by doubling the sum of one plus the value programmed.

▶ Interlace Sync and Video Mode

The total number of rasters in the character format is one more than the value parameter, as in the noninterlace mode, but the rasters alternate fields. In the following tabulation, a value parameter of 4 is set.

RASTER ADDRESS	RESULTING FORMAT
0	- - - - - - -
1	. . . .
2	- - - - - - -
3	. . . .
4	- - - - - - -

NOTE: - - - - - - - and . . . . . denote alternate fields.

CURSOR START RASTER REGISTER (R10)

RIO programs the cursor-start raster (line) address and the cursor-display mode. The lower 5 bits (D0-D4) are cursor-start, and the next 2 bits (D5, D6) are cursor-mode.

Table D-7: Cursor Display Mode (D6, D5)

D5	D6	CURSOR DISPLAY MODE
0	0	Steady cursor
0	1	Cursor off
1	0	Blinking cursor, 16-field period
1	1	Blinking cursor, 32-field period

CURSOR END RASTER REGISTER (R11)

R11 sets the cursor-end raster (line) address.

START ADDRESS REGISTERS (R12, R13)

R12 and R13 are used to program the first (word) address of the screen buffer memory to be displayed. This word will display as line one/column one on the display screen.

CURSOR REGISTERS (R14, R15)

The two read/write registers R14 and R15 store the cursor location. The upper 2 bits (D6, D7) of R14 must always be set to "0".

LIGHT PEN REGISTERS (R16, R17)

The read-only registers R16 and R17 are used to latch the detection-time address of the light pen. The upper 2 bits (D6, D7) of R16 are always "0". The value latched may need to be corrected by software to allow for light pen system delays.

RESTRICTIONS ON PROGRAMMING INTERNAL REGISTERS

The following restrictions on programming internal registers apply:

- 0†Nhd†(Nht + 1)†=256
- 0†Nvd†(Nvt + 1)†=128
- 0†=Nhsp†=Nht
- 0†=Nvsp†=Nvt*
- 0=†NCSTART=†NCEND=†Nr (noninterlace, interlace sync mode)
  0=†NCSTART†NCEND=†Nr+1 (interlace sync and video mode)
- 2=†Nr=†30
- 3=†Nht (except non interlace mode)
  5=†Nht (noninterlace mode only)

*In interlace mode, pulse width is changed +1/2 by the raster time when the vertical sync signal extends over two fields.

NOTES: The values programmed in the internal registers of the CRTC are used directly to control the CRT. Consequently, the display may flicker if the contents of the registers are changed asynchronously to the display operation. The registers should be changed only during the horizontal or vertical retrace period.

NONINTERLACE MODE DISPLAY

Alternate fields are identical. The values of raster addresses (RA0-RA4) are counted, starting at zero.

INTERLACE SYNC MODE DISPLAY

In the interlace sync mode, raster addresses in the even field and the odd field are the same. The same character pattern is displayed in both fields with the displayed position in the odd field 1/2 raster space down from that in the even field.

INTERLACE SYNC AND VIDEO MODE DISPLAY

In interlace sync and video mode, when the raster number is even, the output raster address is different from when the raster number is odd.

Table D-8: Programmed Values into the Registers

REGISTER	REGISTER NAME	VALUE
R0	Horizontal total	Nht
R1	Horizontal displayed	Nhd
R2	Horizontal sync position	Nhsp
R3	Sync width	Nvsw, Nhsw
R4	Vertical total	Nvt
R5	Vertical total adjust	Nadj
R6	Vertical displayed	Nvd
R7	Vertical sync position	Nvsp
R8	Interlace and skew	
R9	Maximum raster address	Nn
R10	Cursor start raster	
R11	Cursor end raster	
R12	Start address (H)	0
R13	Start address (L)	0
R14	Cursor (H)	
R15	Cursor (L)	
R16	Light pen (H)	
R17	Light pen (L)	

NOTE: Nhd†Nht, Nvd†Nvt

Table D-9: Output Raster Address in Interlace Sync and Video Mode

TOTAL NUMBER OF RASTERS IN THE CHARACTER FORMAT	FIELD	
	EVEN	ODD
Even	Even Address	Odd Address
Odd		
Even Line	Even Address	Odd Address
Odd Line	Odd Address	Even Address

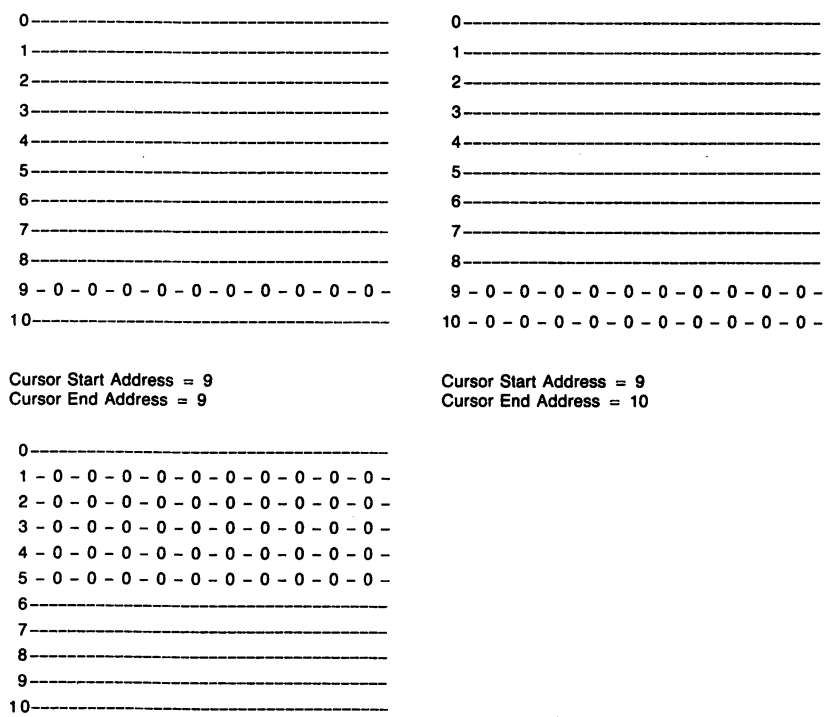
NOTE: Internal line address begins from zero.

NOTE: A wide disparity in the number of ON dots in even fields versus that in odd fields causes unequal average beam currents during alternate fields. This causes CRT final-anode voltage to differ during alternate fields. Since the deflection factor is a function of this voltage, the two fields will have somewhat different widths. Characters will be distorted, particularly near the edges of the screen. Programming for an odd number of rasters per character line is a good way to reduce this type of problem.

CURSOR CONTROL

Figure D-3 shows display patterns in which various values are stored in the cursor-start-raster register and the cursor-end-raster register. Values in the cursor-start-raster register and the cursor-end-raster register must meet the following conditions: cursor-start-raster†= cursor end raster register†= maximum raster address.

Figure D-3: Cursor Control



Audio output from and (optionally) input to the system are provided by a built-in coder/decoder (CODEC), which uses a Continuously-Variable-Slope Delta modulation (CVSD) technique. This device produces audio output by converting a single-bit, digital-bit stream to an analog output.

The bit-stream interface is provided by the 6852-SSDA chip which converts 8-bit data bytes from the processor to a bit-serial data stream for the CODEC. The SSDA also provides encode/decode control, via the DTR output, and a 3-byte FIFO buffer which reduces the real-time processor servicing requirements.

Additional control of the audio section is provided by VIA 1 and VIA 3. The signals provided are Codec Clock and Volume Control. The encode/decode line, controlled by DTR from the SSDA, selects the desired audio function (input or output). Codec clock is a PB7 output (of VIA 3), a timer-generated signal which determines Codec sampling rate (normally about 16KHz). Volume control, a CB2 output (of VIA 1), is a timer-controlled recirculating shift register output and is an eight-step, pulse-width-modulated ultra-audio signal.

INPUT SIGNAL CONDITIONING

The microphone amplifier utilizes half of an LM358 and a JFET in a variable-gain amplifier used as a compressor. The attack time of the compressor is about 50 milliseconds; release time is 250 mS. Input signal amplitude range for acceptable record quality is about 5 to 75 mVRMS. The second stage, 1/2 of a LM358, is a 3-pole butterworth low-pass filter with a cutoff-frequency of about 3 KHz. This filter eliminates "aliasing" in the CVSD modulator.

OUTPUT CONDITIONING AND POWER AMPLIFIER

Following the CVSD, the output (playback) signal is low-pass filtered by another active, 3 KHz cutoff butterworth filter (1/4 LM324). Following this stage, a CA4066B and its attendant drivers provide software-controlled volume control by varying the duty-factor of signal CODEC VOL. The frequency of this signal (including the produced sidebands) must be high enough to be above audible range; a minimum of 20 KHz is recommended. Playback power amplification is provided by an LM383. This stage also provides some roll-off to alleviate the above problem. The power stage will produce 4 watts of audio; thus, an external speaker should be used if above-normal sound levels are programmed, since the internal speaker is rated at only 300 milliwatts.

SSDA DEVICE OPERATION

OVERVIEW

At the bus interface, the SSDA appears as two addressable memory locations. Internally, there are seven registers: two read-only and five write-only registers. The read-only registers are Status and Receive Data; the write-only registers are Control 1, Control 2, Control 3, Sync-Code and Transmit Data. The serial interface consists of serial input and output lines with independent clocks and four peripheral/modem control lines.

Data to be transmitted is transferred directly into the 3-byte Transmit Data First-In First-Out (FIFO) register from the data bus. Availability of the input to the FIFO is indicated by a bit in the Status register; once data is entered, it moves through the FIFO to the last empty location. Data at the output of the FIFO is automatically transferred from the FIFO to the Transmitter Shift register as the shift register becomes available to transmit the next character. If data is not available from the FIFO (underflow condition), the Transmitter Shift register is automatically loaded with either a sync code or an all 1's character. The transmit section should be programmed to not append parity onto the transmitted word.

For use in the S1 audio system, the SSDA should normally be programmed to use 8-bit, no parity, and External Sync mode. Then the DTR control selects the input or output function. However, for completeness and any special functions, all modes of SSDA operation are discussed in the following sections.

The method of serial data accumulating in the receiver depends on the synchronization mode selected. In External Sync mode, used for parallel-serial operation, the receiver is synchronized by the DCD (Data Carrier Detect) input and transfers successive bytes of data to the input of the Receiver FIFO. The Single-Sync-Character mode requires a match between the Sync-Code register and one incoming character before data transfer to the FIFO begins. In Two-Sync-Character mode, two sync codes must be received in sequence to establish synchronization. Subsequent to synchronization in any mode, data is accumulated in the shift register. Availability of a word at the FIFO output is indicated by a bit in the Status register.

The SSDA and its internal registers are selected by the address bus and the Read/Write (R/W) and Enable control lines. To configure the SSDA, Control registers are selected and the appropriate bits set. The Status register can be selected to read status.

The transmitter and receiver clock inputs are tied together. Signals to the microprocessor are the Data bus and Interrupt Request (IRQ).

INITIALIZATION

During a power-up sequence, system reset sets the SSDA in an internally-latched reset condition to prevent erroneous output transitions. The Sync-Code register, Control register 2, and Control register 3 should be loaded prior to the programmed release of the Transmitter and/or Receiver Reset bits. The bits in Control register 1 should be cleared after the Reset line has gone high.

TRANSMITTER OPERATION

Data is transferred to the transmitter section in parallel form via the data bus and the Transmit Data FIFO. The Transmit Data FIFO is a 3-byte register whose status is indicated by the Transmitter Data Register Available status bit (TDRA) and its associated interrupt enable bit. Data is transferred through the FIFO on negative edges of PHASE2 pulses. Two data transfer modes are provided in the SSDA: the 1-byte transfer mode provides for writing data to the transmitter section (and reading from the receiver section) one byte at a time; the 2-byte transfer mode provides for writing two data characters in succession.

Data automatically transfers from the last register location in the Transmit Data FIFO (when it contains data) to the Transmitter Shift register during the last half of the last bit of the previous character. A character is transferred into the Shift register by the Transmitter Clock. Data is transmitted LSB first.

When the Shift register becomes empty and data is not available for transfer from the Transmit Data FIFO, an underflow results, and a character is inserted into the transmitter data stream. This character will be either all 1's or the contents of the Sync-Code register, depending on the state of the Transmit Sync-Code-On-Underflow control bit.

Transmission is initiated by clearing the Transmitter Reset bit in Control register 1. When the Transmitter Reset bit is cleared, the first full positive half-cycle of the Transmit Clock initiates the transmit cycle; the transmission of data (or underflow characters) begins on the negative edge of the Transmit Clock pulse which started the cycle. If the Transmit Data FIFO has not been loaded, an underflow character is transmitted. When the Transmitter Reset bit (Tx Rs) is set, the Transmit Data FIFO is cleared and the TDRA status bit is cleared. After one PHASE2 clock has occurred, the Transmit Data FIFO becomes available for new data and TDRA is inhibited.

RECEIVER OPERATION

Data and a pre-synchronized clock are provided to the SSDA receiver section by means of the Receive Data (Rx Data) and Receive Clock (Rx Clk) inputs. The data is a continuous bit stream; character boundaries cannot be identified within the stream. The Receiver Shift register outputs are high when it is in the reset state.

SYNCHRONIZATION

The SSDA provides three operating modes related to character synchronization: One-Sync-Character mode, Two-Sync-Character mode, and External Sync mode. The External Sync mode requires synchronization and control of the receiving section through the Data Carrier Detect (DCD) input. The external synchronization source could consist of a direct control line from the transmitting end of the serial data link or from external logic designed to detect the start of a message block. The One-Sync-Character mode searches on a bit-by-bit basis until a match is achieved between the data in the Shift register and the Sync-Code register. A match indicates that character synchronization is complete and will be retained for the message block. In the Two-Sync-Character mode, the receiver searches for the first sync-code match on a bit-by-bit basis and then looks for a second successive sync-code character prior to establishing character synchronization. If the second sync-code character is not received, the bit-by-bit search for the first sync-code resumes.

Sync-codes received prior to the completion of synchronization (one or two character) are not transferred to the Receive Data FIFO. Redundant sync-codes received during the preamble or sync-codes which occur as fill characters can automatically be stripped from the data by setting the Strip-Sync control bit to minimize system loading. Character synchronization is retained until cleared by means of the Clear-Sync bit. This bit also inhibits the synchronization search routine.

RECEIVING DATA

Once synchronization has been achieved, subsequent characters are automatically transferred into the Receive Data FIFO and clocked through the FIFO to the last empty location by PHASE2 pulses. The Receiver Data Available status-bit (RDA) indicates when data is available to be read from the last FIFO location (number 3) when in the 1-byte transfer mode. The 2-byte transfer mode causes the RDA status bit to indicate that data is available when the last two FIFO register locations are full. Available data in the Receive Data FIFO triggers an interrupt request if the Receiver Interrupt Enable bit (RIE) is set. The CPU should then read the SSDA Status register, which indicates whether data is available for the CPU to read from the Receive Data FIFO register. The IRQ and RDA status bits are reset by a read from the FIFO.

If more than one character has been received and is resident in the Receive Data FIFO, subsequent PHASE2 clocks cause the FIFO to update and the RDA and IRQ status-bits to again be set. The read-data operation for the 2-byte transfer mode requires a PHASE2 clock intervening between reads to allow the FIFO data to shift.

The other status bit which pertains to the receiver section is Receiver Overrun. The Overrun status bit is automatically set when a character is transferred to the Receive Data FIFO while the first register of the Receive Data FIFO is full. Overrun causes an interrupt if Error Interrupt Enable (EIE) has been set. The transfer of the overrunning character into the FIFO causes the previous character in the FIFO input register location to be lost. The Overrun status bit is cleared by reading the Status register (when the overrun condition is present) followed by a Receive Data FIFO register read. Overrun cannot occur and be cleared without providing an opportunity to detect its occurrence via the Status register.

INPUT/OUTPUT FUNCTIONS

SSDA INTERFACE SIGNALS FOR CPU

The SSDA interfaces to the CPU with an 8-bit bidirectional data bus (ID0-ID7), a chip-select line, a register-select line, an interrupt-request line, a read/write line, an enable line, and a reset line. These signals permit the CPU to have complete control over the SSDA.

SSDA Bidirectional Data (ID0-ID7)

The bidirectional data lines (D0-D7) allow for data transfer between the SSDA and the CPU. The data bus output drivers are three-state devices that remain in the high-impedance (off) state except when the CPU performs an SSDA read operation.

SSDA Enable (PHASE2)

The Enable signal, PHASE2, is a high impedance TTL-compatible input that enables the bus input/output data buffers, clocks data to and from the SSDA, and moves data through the FIFO Registers. This signal is the continuous System PHASE2 1 Mhz clock.

Read/Write (R/W)

The Read/Write line is a high-impedance input that is TTL-compatible and is used to control the direction of data flow through the SSDA's input/output data bus interface. When Read/Write is high (CPU read cycle), SSDA output drivers are turned on if the chip is selected and a selected register is read. When it is low, the SSDA output drivers are turned off and the CPU writes into a selected register. The Read/Write signal is also used to select read-only or write-only registers within the SSDA.

Chip Select (CS)

The Chip Select line is a high impedance TTL-compatible input line used to address the SSDA. The SSDA is selected when CS is low. Transfers of data to and from the SSDA are performed under the control of the Enable signal, Read/Write, and Register Select.

Register Select (RS)

The Register Select line is a high impedance input that is TTL-compatible. A high level is used to select Control registers C2 and C3, the Sync Code register, and the Transmit/Receive Data registers. A low level selects the Control 1 and Status registers (see Table 1). This line is driven by the A0 bit of the system address bus.

Interrupt Request (IRQ)

Interrupt Request is a TTL-compatible, open-drain (no internal pullup), active-low output that is used to interrupt the CPU. The Interrupt Request remains low until cleared by the CPU.

Reset Input

The Reset input provides a means of resetting the SSDA from an external source. In the low state, the Reset input causes the following:

- The Receiver Reset (Rx Rs) and Transmitter Reset (Tx Rs) bits are set, causing both the receiver and transmitter sections to be held in a reset condition.
- Peripheral Control bits PC1 and PC2 are reset to zero, causing the SM/DTR output to be high.
- The Error Interrupt Enable (EIE) bit is reset.
- An internal synchronization mode is selected.
- The Transmitter Data Register Available (TDRA) status bit is cleared and inhibited.

When Reset returns high (the inactive state), the transmitter and receiver sections remain in the reset state until the Receiver Reset and Transmitter Reset bits are cleared via the bus under software control. The Control Register bits affected by Reset (Rx Rs, Tx Rs, PC1, PC2, EIE, and E/I Sync) cannot be changed when Reset is low.

CLOCK INPUTS

Separate high impedance TTL-compatible inputs are driven by a common source for clocking transmitted and received data. The source is the CB2 signal from the Control Port VIA.

Transmit Clock (Tx Clk)

The Transmit clock input is used to clock out of transmitted data. The transmitter shifts data on the negative transition of the clock.

Receive Clock (Rx Clk)

The Receive clock input is used to clock in received data. The clock and data must be synchronized externally. The receiver samples the data on the positive transition of the clock.

SERIAL INPUT/OUTPUT LINES

Receive Data (Rx Data)

The Receive Data line is a high impedance TTL-compatible input through which data is received in a serial format. Data rates may be from 0 to 600 kbs.

Transmit Data (Tx Data)

The Transmit Data output line transfers serial data to a modem or other peripheral. Data rates may be from 0 to 600 kbs.

SSDA REGISTERS

Seven registers in the SSDA can be accessed by means of the bus. The registers are defined as read-only or write-only according to the direction of information flow. The Register Select input (RS) selects two registers in each state, one being read-only and the other write-only. The Read/Write input (R/W) defines which pair is actually accessed. Four registers (two read-only and two write-only) can be addressed via the bus at any particular time. These registers and the required adressing are defined in Table E-1.

Table E-1: SSDA Programming Model

	INPUTS		CONTROL		REGISTER CONTENT							
REGISTER	RS	R/W	AC2	AC1	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Status (S)	0	1	X	X	Interrupt Request (IRQ)	Receiver Parity Error	Receiver Overrun (RX Ovrn)	Transmitter Underflow (TUF)	Clear-to-Send ($\overline{CTS}$)	Data Carrier Detect ($\overline{DCD}$)	Transmitter Data Register Available (TDRA)	Receiver Data Available (RDA)
Control (C1)	0	0	X	X	Address Control 2 (AC 2)	Address Control 1 (AC 1)	Receiver Interrupt Enable (RIE)	Transmitter Interrupt (TIE)	Clear Sync	Strip Sync Characters (Strip Sync)	Transmitter Reset (Tx Rs)	Receiver Reset (Rx Rs)
Receive Data FIFO	1	1	X	X	D7	D6	D5	D4	D3	D2	D1	D0
Control 2 (C2)	1	0	0	0	Error Interrupt Enable (EIE)	Transmit Sync Code on Underflow (TX Sync)	Word Length Select 3 (WS 3)	Word Length Select 2 (WS 2)	Word Length Select 1 (WS 1)	1-Byte/2-Byte Transfer (1-Byte/ 2-Byte)	Peripheral Control 2 (PC 2)	Peripheral Control 1 (PC 1)
Control 3	1	0	0	1	Not Used	Not Used	Not Used	Not Used	Clear Transmitter Underflow Status (CTUF)	Clear $\overline{CTS}$ Status (Clear $\overline{CTS}$)	One-Sync-Character/ Two-Sync-Character Mode Control (1 Sync/ 2 Sync)	External/ Internal Sync Mode Control (E/I Sync)
Sync Code	1	0	1	0	D7	D6	D5	D4	D3	D2	D1	D0
Transmit	1	0	1	1	D7	D6	D5	D4	D3	D2	D1	D0

X = Don't care.

CONTROL REGISTER 1 (C1)

Control register 1 is an 8-bit write-only register that can be directly addressed from the data bus. Control register 1 is addressed when RS equals zero.

Receiver Reset (Rx Rs), C1 Bit 0

The Receiver Reset control bit provides both a reset and inhibit function to the receiver section. When Rx Rs is set, it clears the receiver control logic, sync logic, error logic, Rx Data FIFO Control, Parity Error status bit, and DCD interrupt. The Receiver Shift register is set to "ones." The Rx Rs bit must be cleared after the occurrence of a low level on Reset in order to enable the receiver section of the SSDA.

Transmitter Reset (Tx Rs), C1 Bit 1

The Transmitter Reset control bit provides both a reset and inhibit to the transmitter section. When Tx Rs is set, it clears the transmitter control section, Transmitter Shift register, Tx Data FIFO Control (the Tx Data FIFO can be reloaded after one PHASE2 clock pulse), the Transmitter Underflow status bit, and the CTS interrupt, and inhibits the TDRA status bit (in the one-sync-character and two-sync-character models). The Tx Rs bit must be cleared after the occurrence of a low level on Reset in order to enable the transmitter section of the SSDA. If the Tx FIFO is not preloaded, it must be loaded immediately after the Tx Rs release to prevent a transmitter underflow condition.

Strip Synchronization Characters (Strip-Sync), C1 Bit 2

If the Strip-Sync bit is set, the SSDA automatically strips all received characters which match the contents of the Sync-Code register. The characters used for synchronization (one or two characters of sync) are always stripped from the received data stream.

Clear Synchronization (Clear-Sync), C1 Bit 3

The Clear-Sync control bit provides the capability of dropping receiver character synchronization and inhibiting resynchronization. The Clear-Sync bit is set to clear and inhibit receiver synchronization in all modes and is reset to zero to enable resynchronization.

Transmitter Interrupt Enable (TIE), C1 Bit 4

TIE enables both the Interrupt Request output (IRQ) and Interrupt Request status bit to indicate a transmitter service request. When TIE is set and the TDRA status bit is high, the IRQ output goes low (the active state), and the IRQ status bit goes high.

Receiver Interrupt Enable (RIE), C1 Bit 5

RIE enables both the Interrupt Request output (IRQ) and the Interrupt Request status bit to indicate a receiver service request. When RIE is set and the RDA status bit is high, the IRQ output goes low (the active state), and the IRQ status bit goes high.

Address Control 1 (AC1) and Address Control 2 (AC2), C1 Bits 6 and 7

AC1 and AC2 select one of the write-only registers (Control 2, Control 3, Sync-Code, or Tx Data FIFO), as shown in Table G-1, when RS equals one and R/W equals zero.

CONTROL REGISTER 2 (C2)

Control register 2 is an 8-bit write-only register which can be programmed from the bus when the Address Control bits in Control register 1 (AC1 and AC2) are reset and RS equals one and R/W equals zero.

Peripheral Control 1 (PC1) and Peripheral Control 2 (PC2), C2 Bits 0 and 1

The Peripheral Control 1 bit (PC1) and the Peripheral Control 2 bit (PC2) control the direction of data transfer and the selected CODEC function (Encode for receive; Decode for transmit). Control is accomplished by setting PC2 and setting PC1 to 00 for enabling the input (receive) function or to a 01 to enable the output (transmit) function. The DTR output is connected directly to the CTS input of the SSDA. Its complement is connected to the DCD input of the SSDA, as well as to the Encode/Decode select (pin 10) of the CODEC.

1-Byte/2-Byte Transfer (1-Byte/2-Byte), C2 Bit 2

When 1-Byte/2-Byte is set, the TDRA and RDA status bits indicate the availability of their respective data FIFO registers for a single byte data transfer. If 1 Byte/2 Byte is reset, the TDRA and RDA status bits indicate when two bytes of data can be moved without a second status-read. An Enable pulse must occur between data transfers.

Word Length Selects (WS1, WS2, WS3), C2 Bits 3, 4, and 5

Word Length Select bits WS1, WS2, and WS3 select the word length (including parity) for the 7, 8, and 9 bits, as shown in Table G-1.

Transmit Sync-Code on Underflow (Tx Sync), C2 Bit 6

When Tx Sync is set, the transmitter automatically sends a sync-character when data is not available for transmission. If Tx Sync is reset, the transmitter transmits a Mark character (including the parity bit position) on underflow. If the Tx Sync bit is set when the underflow is detected, a pulse approximately the width of a Tx Clk high-period occurs on the underflow output. Internal parity generation is inhibited during underflow except for sync-code fill-character transmission in 8-bit-plus parity word lengths.

Error Interrupt Enable (EIE), C2 Bit 7

When EIE is set, the IRQ status bit goes high and the IRQ output goes low if —

- A receiver overrun occurs. The interrupt is cleared by reading the Status Register and reading the Rx Data FIFO.
- The transmitter has underflowed (in the Tx Sync On Underflow Mode). The interrupt is cleared by writing a "1" into the Clear Underflow, C3 bit 3, or Tx Reset.

When EIE is a 0, the IRQ status bit and the IRQ output are disabled for the preceding error conditions. A low level on the Reset input resets EIE to "0."

CONTROL REGISTER 3 (C3)

Control register 3 is a 4-bit write-only register that can be programmed from the bus when RS equals one and R/W equals zero and when Address Control bits AC1 equals one and AC2 equals zero.

External/Internal Sync Mode Control (E/1 Sync), C3 Bit 0

When the E/1 Sync Mode bit is high, the SSDA is in External Sync mode, and the receiver synchronization logic is disabled. Synchronization can be achieved by means of the DCD input. The DCD input is controlled directly by the DTR output, whose operation is described earlier in "Control Register 2, bits PCO and PC1." Both the transmitter and receiver sections operate as parallel-to-serial converters in External Sync mode. The Clear-Sync bit in Control register 1 acts as a receiver sync inhibit when high to provide a bus-controllable inhibit. The Sync-Code Register can serve as a

transmitter fill-character register and a receiver match register in this mode. A low on the Reset input resets the E/1 Sync Mode bit, placing the SSDA in Internal Sync mode.

One-Sync-Character/Two-Sync-Character Mode Control (1 Sync/2 Sync), C3 Bit 1

When the 1 Sync/2 Sync bit is set, the SSDA synchronizes on a single match between the received data and the contents of the Sync-Code register. When the 1 Sync/2 Sync bit is reset, two successive sync characters must be received prior to receiver synchronization. If the second sync character is not detected, the bit-by-bit search resumes from the first bit in the second character. Refer to the section of the Sync Code register for more detailed description.

Clear CTS Status (Clear CTS), C3 Bit 2

When a "1" is written into the Clear CTS bit, the stored status and interrupt are cleared. Subsequently, the CTS status bit reflects the state of the CTS input. The Clear CTS control bit does not affect the CTS input or its inhibit of the transmitter section. The Clear CTS command bit is self-clearing, so writing a "0" into this bit accomplishes nothing.

Clear Transmit Underflow Status (CTUF), C3 Bit 3

When a "1" is written into the CTUF status bit, the CTUF bit and its associated interrupt are reset. The CTUF command bit is self-clearing.

SYNC-CODE REGISTER

The Sync-Code register is an 8-bit register for storing the programmable sync code required for received data character synchronization in the One-Sync-Character and Two-Sync-Character modes. The Sync-Code register also provides for stripping the sync/fill characters from the received data (a programmable option) and for automatic insertion of fill characters in the transmitted data stream. The Sync-Code register is not used for receiver character synchronization in the External Sync mode; instead, it provides storage of receiver match and transmit fill characters.

The Sync-Code register can be loaded when AC2 and AC1 are a "1" and a "0", respectively, and if R/W equals zero and RS equals one.

The Sync-Code Register may be changed after the detection of a match with the received data (the first sync-code having been detected) to synchronize with a double-word sync pattern. (This sync-code change must occur prior to the completion of the second character.) The sync-match (SM) output can be used to interrupt the CPU system to indicate that the first eight bits have matched. The service routine would then change the Sync Code register to the second half of the pattern. Alternately, One Sync-Character mode can be used for sync-codes of more than 8 bits by using software to check the second and subsequent bytes after reading them from the FIFO.

PARITY FOR SYNC CHARACTER

The Transmitter does not generate parity for the sync character except in 9-bit mode:

Transmitter

9-bit (8-bit + parity) generates an 8-bit sync character + parity

8-bit (7-bit + parity) generates an 8-bit sync character (no parity)

7-bit (6-bit + parity) generates a 7-bit sync character (no parity)

Receiver

DURING SYNCHRONIZATION The Receiver automatically strips the sync character(s) (there are two sync characters if 2-sync mode is selected) used to establish synchronization. Parity is not checked for these sync characters.

AFTER SYNCHRONIZATION IS ESTABLISHED When the "strip-sync" bit is selected, the sync characters (fill characters) are stripped, and parity is not checked for the stripped sync (fill) characters. When the strip-sync bit is not selected (low), the sync character is assumed to be normal data and is transferred into FIFO after parity checking (if a parity format is selected).

Table E-2: Strip Sync Control Bit

STRIP SYNC (C1 BIT 2)	WSO-WS2 (DATA FORMAT; C2 BIT 3-5)	OPERATION
1	X	No transfer of sync-code. No parity check of sync-code.
0	With parity	*Transfer data and sync-codes. Parity check.
0	Without parity	*Transfer data and sync-codes. No parity check.

*Subsequent to synchronization.

Care should be exercised in selecting the sync character in the following situations:

- When Data format is (6 + parity) or (7 + parity)
- When Strip sync is not selected (low)
- When sync code is used as a fill character, and synchronization is established

The transmitter sends a sync character with parity, but the receiver checks the parity as if it were normal data. Therefore, the sync character should be chosen to match the parity check selected for the receiver in the special cases described in Table E-2.

RECEIVE DATA FIRST-IN FIRST-OUT REGISTER (Rx Data FIFO)

The Receive Data FIFO register consists of three 8-bit registers and is used for buffer storage of received data. Each 8-bit register has an internal status bit that monitors its full or empty condition. Data is always transferred from a full register to an adjacent empty register. The transfer from register to register occurs on PHASE2 pulses. The RDA status bit is high when data is available in the last location of the Rx Data FIFO.

In an Overrun condition, the overrunning character is transferred into the full first stage of the FIFO register and causes the loss of that data character. Successive overruns continue to overwrite the first

register of the FIFO. This destruction of data is indicated by the Overrun status bit. The Overrun bit is set when the overrun occurs and remains set until the Status Register is read and a read of the Rx Data FIFO occurs.

Unused data bits for short word lengths (including the parity bit) appear as zeros on the data bus when the Rx Data FIFO is read.

TRANSMIT DATA FIRST-IN FIRST-OUT REGISTER (TX DATA FIFO)

The Transmit Data FIFO register consists of three Shift registers used for buffer storage of data to be transmitted. Each 8-bit register has an internal status bit which monitors its full or empty condition. Data is always transferred from a full register to an adjacent empty register. The transfer is clocked by pulses. The TDRA status bit is high if the Tx Data FIFO is available for data.

Unused data bits for short word lengths are handled as "don't cares." The parity bit is not transferred over the data bus since the SSDA generates parity at transmission.

When an Underflow occurs, the Underflow character is either the contents of the sync-code register or an all-ones character. The Underflow is stored in the Status register until cleared and appears on the Underflow output as a pulse approximately the width of a Tx Clk high period.

STATUS REGISTER

The Status register is an 8-bit read-only register. It provides the real-time status of the SSDA and the associated serial data channel. Reading the Status register is nondestructive. The method of clearing status bits depends upon the function each bit represents and is treated separately for each bit in the register, as described in the following sections.

Receiver Data Available (RDA), S Bit 0

The Receiver Data Available status bit indicates when receiver data can be read from the Rx Data FIFO. The presence of Receiver data is in the last register (#3) of the FIFO causes RDA bit to be high for the 1-byte transfer mode. In the 2-byte transfer mode, a high RDA bit indicates that the last two registers (#2 and #3) are full. The second character can be read without a second status read (to determine whether the character is available). Status must be read on a byte-by-byte basis if receiver data error checking is desired. The RDA status bit is reset automatically when data is not available.

Transmitter Data Register Available (TDRA), S Bit 1

The TDRA status bit indicates that data can be loaded into the Tx Data FIFO register. An empty first register (#1) of the Tx Data FIFO is indicated by a high-level TDRA status bit in the 1-byte transfer mode. The first two registers (#1 and #2) must be empty for TDRA to be high when in the 2-byte transfer mode. The Tx Data FIFO can be loaded with two bytes without an intervening status read. TDRA is inhibited by the Tx reset or reset. Upon Tx Reset, the Tx Data FIFO is cleared and then released on the PHASE2 clock pulse. The Tx Data FIFO can then be loaded with up to three data characters, even though TDRA is inhibited. This feature allows preloading data prior to the release of Tx Reset. A high-level CTS input inhibits the TDRA status bit in either sync mode (One-Sync-Character mode or Two-Sync-Character mode). CTS does not affect TDRA in External Sync mode. Thus the SSDA is allowed to operate under the control of the

CTS input with TDRA indicating the status of the Tx Data FIFO. The CTS input does not clear the Tx Data FIFO in any operating mode.

Data Carrier Detect (DCD), S Bit 2

A positive transition on the DCD input is stored in the SSDA until cleared by reading both Status and Rx Data FIFO. A "1" written into Rx Rs also clears the stored DCD status. The DCD status bit, when true, indicates that the DCD input has gone high. The reading of both Status and Receive Data FIFO allows Bit 2 of subsequent Status reads to indicate the state of the DCD input until the next positive transition.

Clear-to-Send (CTS), S Bit 3

A positive transition on the CTS input is stored in the SSDA until cleared by writing a "1" into the Clear CTS control bit or the Tx Rs bit. The CTS status bit, when true, indicates that the CTS input has gone high. The Clear CTS command (a "1" into C3 Bit 2) allows Bit 3 of subsequent Status reads to indicate the state of the CTS input until the next positive transition.

Transmitter Underflow (TUF), S Bit 4

When data is not available for the transmitter, an underflow occurs and is so indicated in the Status register (in the Tx Sync on underflow mode). The underflow status bit is cleared by writing a "1" into the Clear Underflow (CTUF) control bit or the Tx Rs bit. TUF indicates that a sync character will be transmitted as the next character. A TUF is indicated on the output only when the contents of the Sync-Code Register is to be transferred (transmit sync code on underflow equals one).

Receiver Overrun (Rx Ovrn), S Bit 5

Overrun indicates that data has been received when the Rx Data FIFO is full, resulting in data loss. The Rx Ovrn status bit is set when Overrun occurs. The Tx Ovrn status bit is cleared by reading Status followed by reading the Rx Data FIFO or by setting the Rx Rs control bit.

Receiver Parity Error (PE), S Bit 6

The Parity Error status bit indicates that parity for the character in the last register of the Rx Data FIFO did not agree with selected parity. The parity error is cleared when the character to which it pertains is read from the Rx Data FIFO or when Rx Rs occurs. The DCD input does not clear the Parity Error or Rx Data FIFO status bits.

Interrupt Request (IRQ), S Bit 7

The Interrupt Request status bit indicates when the IRQ output is in the active state (IRQ output equals zero). The IRQ status bit is subject to the same interrupt enables (RIE, TIE, and EIE) as the IRQ output. The IRQ status bit simplifies status inquiries for polling systems by providing a single-bit indication of service requests.

STATUS REGISTER

IRQ Bit 7

The IRQ flag is cleared when the source of the IRQ is cleared. The source is determined by the enables in the Control registers. TIE, RIE, EIE.

Bits 6 to 0

Indicate the SSDA status at a point in time, and can be reset as follows:

PE Bit 6 Read Rx Data FIFO, or a "1" into Rx Rs (C1 Bit 0).

Rx Ovrn Bit 5 Read Status and then Rx Data FIFO or a "1" into Rx Rs (C1 Bit 0).

TUF Bit 4 A "1" into CTUF (C3 Bit-3) or into Tx Rs (C1 Bit 1).

CTS Bit 3 A "1" into Clear CTS (C3 Bit 2) or a "1" into Tx Rs (C1 Bit 1).

DCD Bit 2 Read Status and then Rx Data FIFO or a "1" into Rx Rs (C1 Bit 0).

TDRA Bit 1 Write into Tx Data FIFO.

RDA Bit 0 Read Rx Data in FIFO.

CONTROL REGISTER 1

AC2, AC1 Bits 7, 6 Used to access other registers, as shown above.

RIE Bit 5 When "1", enables interrupt on RDA (S Bit 0).

TIE Bit 4 When "1", enables interrupt on TDRA (S Bit 1).

Clear Sync Bit 3 When "1", clears receiver character synchronization.

Strip Sync Bit 2 When "1", strips all sync codes from the received data stream.

Tx Rs Bit 1 When "1", resets and inhibits the transmitter section.

Rx Rs Bit 0 When "1", resets and inhibits the receiver section.

CONTROL REGISTER 2

CTUF Bit 3 When "1", clears TUF (S Bit 4), and IRQ if enabled.

Clear CTS Bit 2 When "1", clears CTS (S Bit 3), and IRQ if enabled.

1 Sync/2 Sync Bit 1 When "1", selects the one-sync-character mode; when "0", selects the two-sync character mode.

E/1 Sync Bit 0 When "1", selects the external sync mode; when "0", selects the internal sync mode.

CONTROL REGISTER 2

EIE Bit 7 When "1", enables the PE, Rx Ovrn, TUF, CTS, and DCD interrupt flags (S Bits 6 through 2).

Tx Sync Bit 6 When "1", allows sync code contents to be transferred on underflow, and enables the TUF Status bit and output. When "0", an all mark character is transmitted on underflow.

WS3, 2, 1 Bits 5 to 3

Table E-3: Word Length Select

BIT 5 WS3	BIT 4 WS2	BIT 3 WS1	WORD LENGTH
0	0	0	6 bits + even parity
0	0	1	6 bits + odd parity
0	1	0	7 bits, no parity
*0	1	1	8 bits, no parity
1	0	0	7 bits + even parity
1	0	1	7 bits + odd parity
1	1	0	8 bits + even parity
1	1	1	8 bits + odd parity

*This is the mode which should always be used.

1-Byte/2-Byte, Bit 2

When "1", enables the TDRA and RDA bits to indicate when a 1-byte transfer can occur; when "0", the TDRA and RDA bits indicate when a 2-byte transfer can occur.

PC2, PC1, Bits 1 and 0

Table E-4: SM/DTR Output Control

BIT 1 PC2S	BIT 0 PC1	SM/DTR OUTPUT AT PIN 5
0	0	1 Select audio output
1	0	0 Select audio input

CODEC DEVICE OPERATION

The Continuously-Variable-Slope-Delta modulator (CVSD) is a simple alternative to more complex conventional conversion techniques in systems requiring digital communication of analog signals. The human voice is analog, but digital transmission of any signal over great distance is attractive. Signal/noise ratios do not vary with distance in digital transmission, and multiplexing, switching, and repeating hardware is more economical and easier to design. However, instrumentation Analog-to-Digital converters do not meet the communications requirements. The CVSD Analog-to-Digital is well suited to the requirements of digital communications and is an economically efficient means of digitizing voice inputs for transmission.

THE DELTA MODULATOR

The innermost control loop of a CVSD converter is a simple delta modulator. A delta modulator consists of a comparator in the forward path and an integrator in the feedback path of a simple control loop. The inputs to the comparator are the analog input signal and the integrator output. The comparator output reflects the sign of the difference between the input voltage and the integrator output. That sign bit is the digital output and also controls the direction of ramp in the integrator. The comparator is normally clocked, producing synchronous and band-limited digital bit-stream.

If the clocked serial bit-stream is transmitted, received, and delivered to a similar integrator at a remote point, the remote integrator output is a copy of the transmitting control loop integrator output. To the extent that the transmitting integrator tracks the input signal, the remote receiver reproduces that input signal. Low-pass filtering at the receiver output eliminates most of the quantizing noise if the clock rate of the bit stream is an octave or more above the upper band limit of the input signal. Input bandwidth cuts off above 3 kHz, so clock rates from 8 kHz up are possible. Thus, the delta modulator digitizes and transmits the analog input to a remote receiver. The serial, unframed nature of the data is ideal for communications networks. With no input at the transmitter, a continuous one/zero alternation is transmitted. If the two integrators are made leaky, then, during any loss of contact, the receiver output decays to zero and receive restart begins without framing when the receiver re-acquires. Similarly, a delta modulator is tolerant of sporadic bit errors.

THE COMPANDING ALGORITHM

The fundamental advantages of the delta modulator are its simplicity and the serial format of its output. Its limitations are those caused by a limited digital bit rate. The analog input must be band-limited and amplitude-limited. The frequency limitations are governed by the Nyquist information rate relationships, and the amplitude capabilities are set by the gain and dynamic range of the integrators.

The frequency limits are bounded on the upper end; that is, for any input bandwidth there exists a clock frequency larger than that bandwidth transmits the signal with a specific noise level. However, the amplitude limits are bounded on both upper and lower ends. For any given signal level, one specific gain achieves an optimum noise level. Unfortunately, the basic delta modulator has a small dynamic range over which the noise level is constant.

The continuously-variable-slope circuitry provides increased dynamic range by adjusting the gain of the integrator. For a given clock frequency and input bandwidth, the additional circuitry increases the delta modulator's dynamic range. External to the basic delta modulator is an algorithm which monitors the past few outputs of the delta modulator in a simple shift register. The register is 2 bits long. The accepted CVSD algorithm simply monitors the contents of the shift register and indicates if it contains all ones or zeros. This condition is called coincidence. When it occurs, it indicates that the gain of the integrator is too small. The coincidence output charges a single pole low-pass filter. The voltage output of this "syllabic filter" controls the integrator gain through a pulse amplitude modulator whose other input is the sign bit or up/down control.

The simplicity of the all-ones/all-zeros algorithm should not be taken lightly. Many other control algorithms using shift registers have been tried. The key to the accepted algorithm is that it provides a measure of the average power or level of the input signal. Other techniques provide more instantaneous information about the shape of the input curve. The purpose of the algorithm is to control the gain of the integrator and to increase the dynamic range. Thus, a measure of the average input level is what is needed.

The algorithm is repeated in the receiver, and thus the level data is recovered in the receiver. Because the algorithm only operates on the past serial data, it changes the nature of the bit stream without changing the channel bit rate.

The effect of the algorithm is to compand the input signal. If the bit stream from a CVSD encoder is played into a basic delta modulator, the output of the delta modulator reflects the shape of the input signal, but all of the output will be at an equal level. Thus, the algorithm is needed at the output to restore the level variations. The bit stream on the channel behaves as if it came from a standard delta modulator with a constant level input.

The delta modulator encoder with the CVSD algorithm provides an efficient method for digitizing voice signals in a manner which is especially convenient for digital communications requirements.

Table E-5: Definitions and Functions of Pins

PIN NUMBER	PIN FUNCTION
Pin 1	VDD (+5 volts)
Pin 2	Audio Ground. Connection to D/A ladders and comparator.
Pin 3	Audio Out. Recovered audio out. Presents approximately 100 kilo-ohm source. Zero signal reference is VDD/2.
Pin 4	AGC (not used). A logic "low" level appears at this output when the recovered signal excursion reaches one-half of full scale value.
Pin 5	Audio Input. Externally AC coupled.
Pin 6	N/C
Pin 7	N/C
Pin 8	Ground Logic Ground
Pin 9	Clock Input
Pin 10	Encode/Decode. A low level selects the encode mode; a high level, the decode mode.
Pin 11	Alternate Plain Text (not used). A low level at this input causes a quieting pattern to be transmitted without affecting the internal operation of the CVSD.
Pin 12	Digital Data Input
Pin 13	Force Zero (not used). A low level at this input forces the transmitted output, the internal logic, and the recovered audio output of the CVSD into the "quieting" condition.
Pin 14	Digital Data Output

MECHANICAL SPECIFICATIONS

KEY TOTAL TRAVEL	Range	.150 in-.200 in ±.010 (3.8 mm-5 mm)	
	Preferred	.170 in (4.3 mm)	
	Key Pretravel (when applicable)	.100 in minimum (2.5 mm)	
ACTUATION FORCE	Standard Key	Range	1.5-2.5 oz ±30% (42.5-70 grams)
		Preferred	1.5 oz ±30% (42.5 grams)
	Special Key	Range	3-5 oz (85-142 grams)
		Preferred	3 oz (85 grams)
RELIABILITY	>100 million cycles		
KEY SPACING	Range	.70-.80 in (18-20 mm)	
	Preferred	.75 in (19 mm)	
KEY SIDEPLAY	.018 in (.5 mm) 2° rotational		
KEY TOP DIMENSION	Range	.47-.60 in (12-15 mm)	
	Preferred	.51 in (13 mm)	
KEY SURFACE	Concave, textured (mat) unless position marked otherwise, low reflection, low glare.		
KEY SWITCH PRESSURES	Keytop shall be capable of withstanding 3 lbs (1.4 kg) pull without coming loose and 11 lbs (5 kg) in the direction of actuation without any damage to the key switch.		

ELECTRICAL SPECIFICATIONS

INPUT POWER	+5VDC ± 5% @ 250 ma
ROLLOVER	N Key
CONNECTOR	Type: AMP 87551-7 or equivalent Spacing: 0.1 in, 7 pin header

Table F-1: Pin Assignment

PIN(S)	NAME	FUNCTION
1, 7	+5V	+5 volts at 250 ma
2, 3	GROUND	System Ground
4	KBACK	TTL Input. Driven by terminal processor. Transitions indicate acknowledgement of KBRDY transitions.
5	$\overline{\text{KBRDY}}$	TTL Output. Driven low by the keyboard to initiate handshake of each data bit of a transmission. Driven high after receipt of the negative edge of the KBACK line.
6	KBDATA	TTL Output. Changed after the positive edge of the KBACK line. Data must change no later than the negative edge of KBRDY. The exception to this is the stop bit. Transfer of the stop bit is as follows: 1) Data line driven low at or before negative edge of KBRDY. 2) Data line and $\overline{\text{KRBDY}}$ driven high following the negative edge of $\overline{\text{KBACK}}$. 3) Keyboard enters the Idle state afterthe positive edge of $\overline{\text{KBACK}}$.

LOGICAL SPECIFICATIONS

PROTOCOL DEFINITION

The communication between the terminal processor and the keyboard is serial. The transmission is in 9-bit words. The first eight bits are the data byte, transmitted LSB first. The last bit is a stop bit.

The keyboard will return key numbers and key status through the eight data bits. The MSB of the key number returned by the keyboard is status which flags a key close or key open. An MSB of one indicates a key close, and an MSB of zero indicates a key open. The least significant 7 bits are the key number.

The stop bit is a zero from $\overline{\text{KBRDY}}$ low to $\overline{\text{KBACK}}$ low. The stop bit goes high before $\overline{\text{KBRDY}}$ goes high and remains high until the next transfer.

The keyboard indicates it has an event in its buffer with the $\overline{\text{KBRDY}}$ line. If transmission is idle, the keyboard can signal an event by taking the $\overline{\text{KBRDY}}$ line low. The high to low transition of $\overline{\text{KBRDY}}$ should flag an interrupt in the terminal processor. The keyboard should raise the $\overline{\text{KBRDY}}$ line on the negative transition of the $\overline{\text{KBACK}}$ line. Each event in the keyboard buffer will cause a transition of the $\overline{\text{KBRDY}}$ line. The keyboard transmission becomes idle after the positive edge of the $\overline{\text{KBACK}}$ line following the stop bit.

The keyboard times out the processor response to $\overline{\text{KBRDY}}$ low for 250 milliseconds. If the processor does not respond with a negative transition of KBACK clock within this time, the keyboard will drive $\overline{\text{KBRDY}}$ high and then restart the current transmission. This will allow the terminal processor to resynchronize to the keyboard data stream.

Table F-2: Switching Characteristics

PARAMETER	FUNCTION DESCRIPTION	REQUIRED TIMING	
		MAX	MIN
TDVRL	KB data valid to KBRDY low	—	0
TRLCL	KBRDY low to KBACK low	250ms	—
TAHKL	KBACK high to KBRDY low (except after stop bit)	1ms	0

RESERVED KEYBOARD CODES

HEX	FUNCTION	DESCRIPTION
FEH	Overflow	Key queue overflow. Keys have been lost.
FFH	Dead	Keyboard dead or not connected.

ENVIRONMENTAL SPECIFICATIONS

OPERATING TEMPERATURE

0° C-50° C

STORAGE TEMPERATURE

-40° C-+60° C

HUMIDITY

0-95% noncondensing

MATERIAL

Self-extinguishable

KEYBOARD APPROVALS

Keyboard meets UL and VDE requirements for approval.

VIBRATION

To be determined

SHOCK

Operating: 10G peak 1/2 sinusoid: 10ms duration
Nonoperating: 100G peak 1/2 sinusoid: 10ms duration

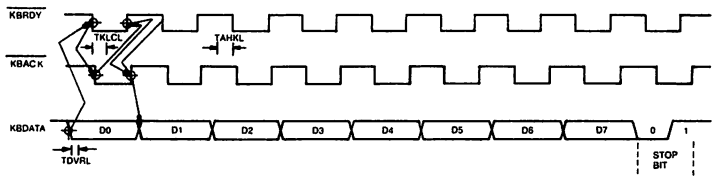
KEYBOARD LAYOUT

Key layouts vary from model to model in relation to the targeted application. The layout is broken into typewriter keys, command keys, and calculator keys. The typewriter pad has 58 possible key positions. The whole keyboard has a total of 104 possible key positions. The typewriter pad is sculptured; other pads are sloped. The layout uses one common PC Board, while the actual number of key positions occupied varies from model to model.

KEYBOARD TIMING DIAGRAM

Figure F-1 illustrates keyboard timing.

Figure F-1: Keyboard Timing Diagram



APPENDIX G COMMUNICATIONS CONTROLLER SPECIFICATIONS

G-1 INTRODUCTION

The NEC uPD7201 Multiprotocol Serial Communications Controller (MPSC²) is a versatile device designed to give you high-level control of your data communication protocols with maximum flexibility and minimum processor overhead. The MPSC² contains two complete full duplex channels in a 40-pin package and incorporates a variety of sophisticated features to simplify your protocol management.

G-1.1 FEATURES

- Implements the three basic data/communications protocols
  - Asynchronous
  - Character-oriented synchronous (monosync, bisync, external sync)
  - Bit-oriented synchronous (SDLC/HDLC)
- Provides extensive error checking
  - Parity
  - CRC-16
  - CRC-CCITT
  - Break/Abort detection
  - Framing Error detection
- Enhanced data reliability
  - Double-buffered transmitters
  - Quadruply-buffered receivers
  - Programmable transmitter underrun handling
- Simplified system design
  - Simple interface to most microprocessors
  - Automatic Interrupt vectoring for most microprocessors
  - Four DMA channels for maximum throughput with standard 8237/8257-type DMA controllers
  - Single-phase TTL clock
  - Single +5 volt supply

G-2 PIN DESCRIPTION

This section describes the various pin functions available on the MPSC². Some pin numbers are used twice because of their programmability and dual functionality. Those pins that have more than one function are marked with an * in the following descriptions. Refer to Section G-5 for detailed information on selecting pin functions.

Figure G-2.1 Functional Pinout

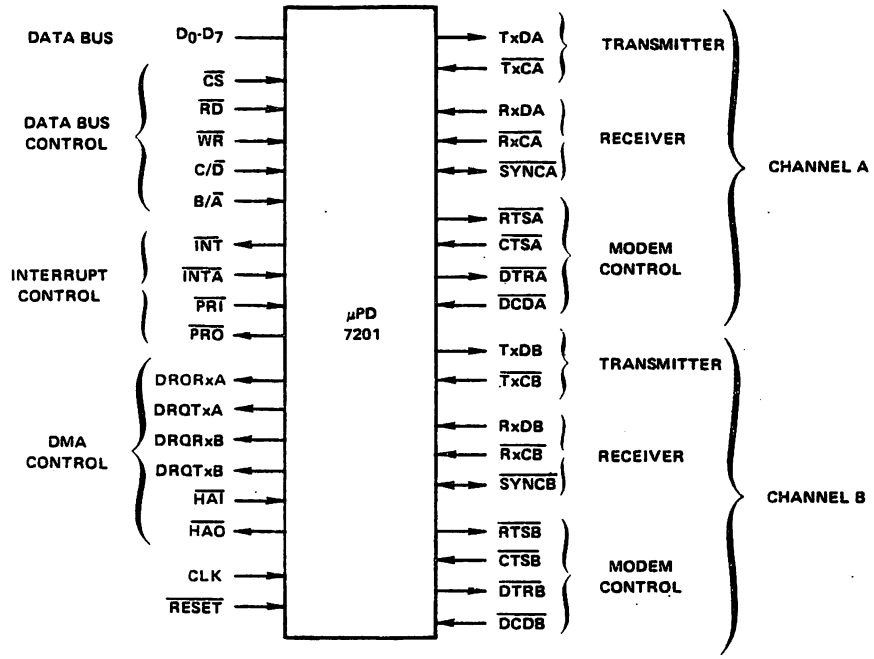
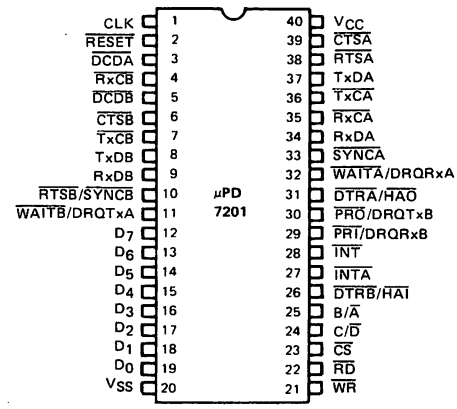


Figure G-2.2 Pin Configuration



12-19 D_0-D_7 Data Bus (bidirectional three-state)
The data bus lines are connected to the system data bus. Data or status from the MPSC² is output on these lines when CS and RD are active and data or commands are latched into the MPSC² on the rising edge of WR when CS is active.

23 CS Chip Select (input, active low)
Chip select allows the MPSC² to transfer data or commands during a read or write cycle.

25 B/A Channel Select (input)
A low selects channel A and a high selects channel B for access during a read or write cycle.

24 C/D Control/Data Select (input)
This input, with RD, WR and B/A, selects the data registers (C/D = 0) on the control and status registers (C/D = 1) for access over the data bus.

22 RD Read (input, active low)
This input (with either CS during a read cycle or HAI during a DMA cycle) notifies the MPSC² to read data or status from the device.

21 WR Write (input, active low)
This input (with either CS during a read cycle or HAI during a DMA cycle) notifies the MPSC² to write data or control information to the device.

2 RESET Reset (input, active low)
A low on this input (one complete CLK cycle minimum) initializes the MPSC² to the following conditions: receivers and transmitters disabled, TxDA and TxDB set to marking (high), and Modem Control Outputs DTRA, DTRB, RTSA, RTSB set high. Additionally, all interrupts are disabled, and all interrupt and DMA requests are cleared. After a reset, you must rewrite all control registers before restarting operation.

1 CLK System Clock (input)
A TTL-level system clock signal is applied to this input. The system clock frequency must be at least 4.5 times the data clock frequency applied to any of the data clock inputs TxCA, TxCB, RxCA or RxCB.

28 INT Interrupt Request (output, open drain, active low)
INT is pulled low when an internal interrupt request is accepted.

27 INTA Interrupt Acknowledge (input, active low)
The processor generates two or three INTA pulses (depending on the processor type) to signal all peripheral devices that an interrupt acknowledge sequence is taking place. During the interrupt acknowledge sequence, the MPSC², if so programmed, places information on the data bus to vector the processor to the appropriate interrupt service location.

29* PRI Interrupt Priority In (input, active low)
This input informs the MPSC² whether the highest priority device is requesting interrupt and is used with PRO to implement a priority resolution "daisy chain" when there is more than one interrupting

device. The state of PRI and the programmed interrupt mode determine the MPSC²'s response to an interrupt acknowledge sequence.

30* PRO Interrupt Priority Out (output, active low)
This output is active when HAI is active and the MPSC² is not requesting interrupt (INT is inactive). The active state informs the next lower priority device that there are no higher priority interrupt requests pending during an interrupt acknowledge sequence.

11*, 32* WAITA WAITB Wait (outputs, open drain)
These outputs synchronize the processor with the MPSC² when block transfer mode is used. You may program it to operate with either the receiver or transmitter, but not both simultaneously. WAIT is normally inactive. For example, if the processor tries to perform an inappropriate data transfer such as a write to the transmitter when the transmitter buffer is full, the WAIT output for that channel is active until the MPSC² is ready to accept the data. The CS, C/D, B/A, RD, and WR inputs must remain stable while WAIT is active.

11*, 29*, 30*, 32* DRQTxA, DRQTxB, DRQRxA, DRQRxB
DMA Request (outputs, active high)
When these lines are active, they indicate to a DMA controller that a transmitter or receiver is requesting a DMA data transfer.

26* HAI Hold Acknowledge In (input, active low)
This input notifies the MPSC² that the host processor has acknowledged the DMA request and has placed itself in the hold state. The MPSC² then performs a DMA cycle for the highest priority outstanding DMA request, if any.

31* HAO Hold Acknowledge Out (output, active low)
This output, with HAI, implements a priority daisy chain for multiple DMA devices. HAO is active when HAI is active and there are no DMA requests pending in the MPSC².

8, 37 TxDA, TxDB Transmit Data (outputs, marking high)
Serial data from the MPSC² is output on these pins.

7, 36 TxCA, TxCB Transmitter Clocks (inputs, active low)
The transmit clock controls the rate at which data is shifted out at TxD. You may program the MPSC² so that the clock rate is 1x, 16x, 32x, or 64x the data rate. Data changes on the falling edge of TxC. TxC features a Schmitt-trigger input for relaxed rise and fall time requirements.

9, 34 RxDA, RxDB Receiver Data (inputs, marking high)
Serial data to the MPSC² is input on these pins.

4, 35 RxCA, RxCB Receiver Clocks (inputs, active low)
The receiver clock controls the sampling and shifting of serial data at RxD. You may program the MPSC² so that the clock rate is 1x, 16x, 32x, or 64x the data rate. RxD is sampled on the rising edge of RxC. RxC features a Schmitt-trigger input for relaxed rise and fall time requirements.

26*, 31* DTRA, DTRB Data Terminal Ready (outputs, active low)
The DTR pins are general-purpose outputs which may be set or reset with commands to the MPSC².

10, 38* RTSA, RTSB Request to Send (outputs, active low)
When you operate the MPSC² in one of the synchronous modes, RTSA and RTSB are general-purpose outputs that you may set or reset with commands to the MPSC². In asynchronous mode, RTS is active immediately as soon as it is programmed on. However, when programmed off, RTS remains active until the transmitter is completely empty. This feature simplifies the programming required to perform modem control.

3, 5 DCDA, DCDB Data Carrier Detect (inputs, active low)
Data carrier detect generally indicates the presence of valid serial data at RxD. You may program the MPSC² so that the receiver is enabled only when DCD is low. You may also program the MPSC² so that any change in state that lasts longer than the minimum specified pulse width causes an interrupt and latches the DCD status bit to the new state.

6, 39 CTSA, CTSB Clear to Send (inputs, active low)
Clear to send generally indicates that the receiving modem or peripheral is ready to receive data from the MPSC². You may program the MPSC² so that the transmitter is enabled only when CTS is low. As with DCD, you may program the MPSC² to cause an interrupt and latch the new state when CTS changes state for longer than the minimum specified pulse width.

10, 33* SYNCA, SYNCB Synchronization (inputs/outputs, active low)
The function of the SYNC pin depends upon the MPSC² operating mode. In asynchronous mode, SYNC is an input that the processor can read. It can be programmed to generate an interrupt in the same manner as DCD and CTS.

In external sync mode, SYNC is an input which notifies the MPSC² that synchronization has been achieved (see Figure G-2.3 for detailed timing). Once synchronization is achieved, hold SYNC low until synchronization is lost or a new message is about to start.

In internal synchronization modes (monosync, bisync, SDLC), SYNC is an output which is active wherever a SYNC character match is made (see Figure G-2.4 for detailed timing). There is no qualifying logic associated with this function. Regardless of character boundaries, SYNC is active on any match.

Figure G-2.3 SYNC Output, External Synchronization

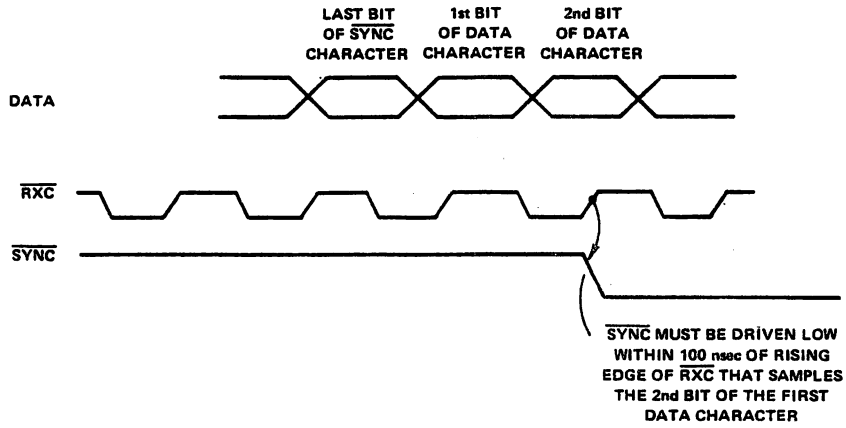
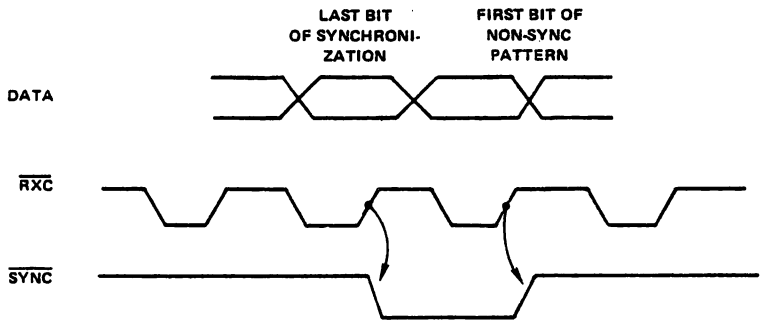


Figure G-2.4 SYNC Output, Internal Synchronization



G-3 PROTOCOLS

A protocol defines a set of rules for transmitting information and control from one place to another. In parallel protocols as you might find on a microprocessor bus, dedicated "control" lines handle functions such as timing, type of information, and error checking. Since the object of serial data communications is to minimize the number of wires, the protocol used must place all of this control information in the serial data stream.

The basic protocol unit or frame can be built into increasingly complex protocols by defining special control characters and fields, and by grouping frames together into larger units. Virtually all communications protocols currently in use are based on one of three basic protocols: Asynchronous, Synchronous Character- or Count-Oriented Protocols (COPs), and Bit-Oriented Protocols (BOPs).

G-3.1 ASYNCHRONOUS PROTOCOL

In asynchronous protocol, each character transmitted has its own framing information in the form of a start and stop bit(s). Each character is a "message" in itself and may be asynchronous with respect to any others. You can implement error detection by adding a parity bit to each character. The transmitter makes the parity bit 1 or 0 so that the character plus parity contains an even or odd number of ones for even parity or odd parity, respectively. Figure G-3.1 illustrates the asynchronous data format.

G-3.2 SYNCHRONOUS CHARACTER ORIENTED PROTOCOLS

In synchronous character-oriented protocols (COPs), the start and stop bits associated with each character are eliminated. A synchronization (sync) character that is not part of the data is transmitted before the data to establish proper framing. The synchronization character is usually 8 or 16 bits long. Monosync and IBM Bisync are typical examples of COPs (Figure G-3.2). Since the framing information is presented only at the beginning, the transmitter must insert fill characters to maintain synchronization. Sync characters are commonly used for this purpose.

As with the asynchronous protocol, a parity bit may be used with each character to provide error checking. A more reliable check is performed by calculating a special 16-bit block check character called a Cyclic Redundancy Check (CRC) for the entire data block and transmitting this character at the end of the data. The most commonly used CRC polynomial for COPs is called CRC-16.

A disadvantage of the character-oriented protocol is having to use special characters such as SYNC to define various portions of a message when you send non-character binary data ("transparent data" in bisync terminology). To do this, you must transmit special DLE sequences and selectively exclude certain characters from the CRC calculation for both the transmitter and receiver. The MPSC^2 features special circuitry to simplify this operation.

G-3.3 SYNCHRONOUS BIT-ORIENTED PROTOCOLS

Synchronous Bit-Oriented Protocols (BOPs) use a special set of rules to distinguish between data and framing characters. This eliminates some of the problems associated with COPs. The most common BOPs in use are the almost-identical HDLC and SDLC protocols shown in Figure G-3.3.

The rules for SDLC (henceforth we will refer only to SDLC although the same information applies to HDLC as well) are quite simple. The basic transmission unit is called a frame and is delineated by a special flag character 01111110 (flags cannot be used as filler like the COP sync character). The data or information field may consist of any number of bits; not necessarily an integral number of n-bit characters. Since data could contain the 01111110 pattern, the transmitter performs the following operation: if five consecutive ones are transmitted, the transmitter inserts a zero bit before the next data bit. Likewise, the receiver must delete any zero that follows five consecutive ones. Six consecutive ones indicate a flag character and eight or more ones indicate a special abort condition.

Error checking is done with a 16-bit CRC character inserted between the end of the information field and the End Of Frame flag. The CRC-CCITT polynomial is generally used. The end of a frame is

determined by counting 16 bits (CRC) back from the End Of Frame flag. Special circuitry in the receiver must inform the processor of the boundary between the end of the information field and the beginning of the CRC when the information field is not an integral number of n-bit characters. The MPSC² performs all of the above functions necessary to implement Bit-Oriented Protocols.

Figure G-3.1 Asynchronous Data Character Format

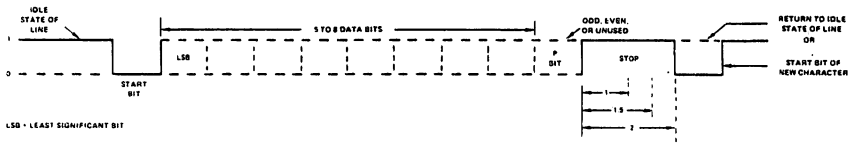


Figure G-3.2 BISYNC Message Format

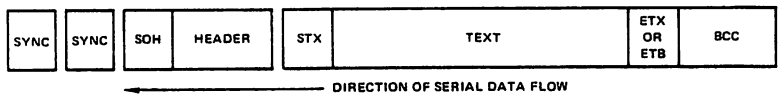
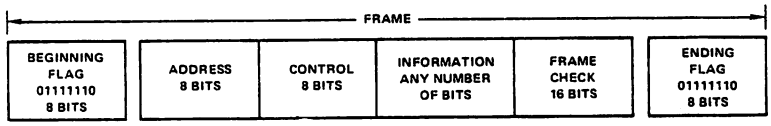


Figure G-3.4 Basic SDLC Frame



G-4 FUNCTIONAL DESCRIPTION

The MPSC² provides two complete serial communications controllers in a single package implementing the following functions:

Parallel-to-Serial and Serial-to-Parallel data conversion.

Buffering of outgoing and incoming data, allowing the processor time to respond.

Insertion and deletion of framing bits and characters.

Calculation and checking of Parity and CRC error checking.

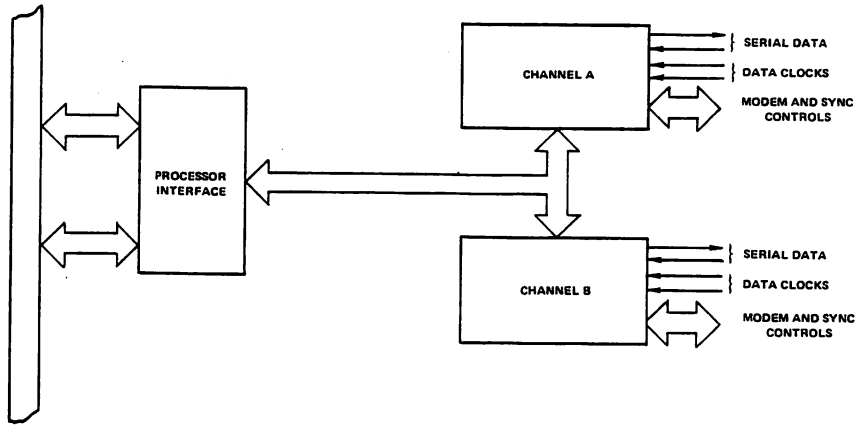
Informing the processor when and what action needs to be taken.

Interfacing with the outside world over discrete modem control lines.

The MPSC² can be logically divided into the following functional groups (Figure G-4.1):

Two identical serial I/O controller channels, each consisting of a Transmitter section and a Receiver section, and a common Processor Interface that connects the MPSC² with the host processor and provides overall device control.

Figure G-4.1 Block Diagram



G-4.1 TRANSMITTER

The MPSC² Transmitter performs all the functions necessary to convert parallel data to the appropriate serial bit streams required by various protocols. The major components of the transmitter are shown in Figure G-4.2. Control and status register fields pertinent to the operation of the transmitter are summarized in Table G-4.1.

The primary data flow through the transmitter begins at the internal data bus. There, characters written to the MPSC² are placed in the buffer register. When any character present in the shift register has been transferred out, or if the shift register is empty, the contents of the buffer register are transferred to the shift register and output with the least significant bit first. Then, a Transmitter Buffer Becoming

Empty indication (flag) is given. This double buffering allows the processor one full character time from this flag to respond with the next character without interrupting data transmission. You should note that it is the transfer of a character from the data buffer to the shift register rather than the empty condition itself that causes the Transmitter Buffer Becoming Empty indication. At initialization or after a Reset Transmitter Interrupt/DMA Pending Command is issued to control register 0 (CR0) you must write one character to the buffer to reset this flag. The Transmitter Buffer Empty bit in status register 0 (SR0), always reflects the presence or absence of a character in the buffer.

After a hardware or software reset, the transmitter data output (TxD) is in high (marking) state. You can pull TxD low (spacing) any time by setting the Send Break bit (CR5 bit 4). TxD remains low until the Send Break bit is reset and any data currently being transmitted is destroyed.

Figure G-4.2 Block Diagram MPSC² Transmitter

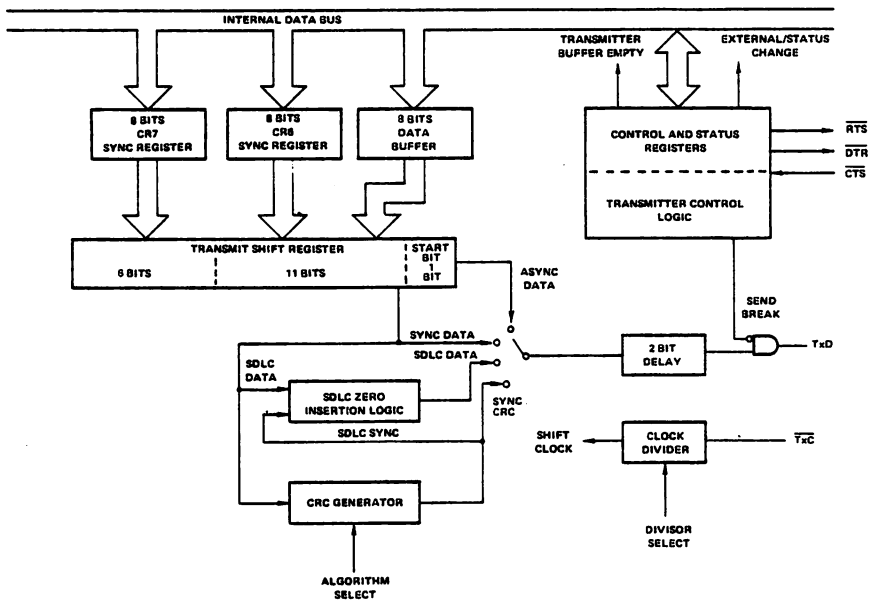


Table G-4.1 Transmitter Control and Status Registers

CONTROL REGISTER	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	CRC CONTROL		COMMAND			REGISTER POINTER		
1							Trans. Int Enable	Ext/Status Int Enable
4	Clock Mode		Sync Format Select		Sync/Async Mode Select		Parity Control	
5	DTR	Bits/Char		Send Break	Transmitter Enable	CRC Type	RTS	CRC Enable
6	SYNC 1							
7	SYNC 2							
3			Auto Enables					

STATUS REGISTER	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0		Trans Underrun/ $\overline{EOM}$	CTS			Trans Buffer Empty		
1								All Async Characters Sent

You can change the number of bits transmitted for each character at any time by modifying the bits/char field (CR5, D_5-D_6) before you load the character into the buffer.

The rate at which data is shifted out is determined by the transmitter clock input (TxC) and the clock mode field (CR4 Bits 6-7). You can select a clock divisor so that the data clock (TxC) rate is equal to 1x, 16x, 32x, or 64x the actual data rate. This field also controls the receiver clock and must be set to 1x for synchronous modes (see Section G-4.2.2 for use in asynchronous mode). Each new bit is shifted out on the falling edge of TxC.

The following is a general discussion of the operation of the MPSC² in various protocol modes. For a detailed description of the registers and examples, see Chapter G-5.

G-4.1.1 Asynchronous Mode

After you select asynchronous mode, initialize the various parameters (number of bits/character, number of stop bits, etc.) and enable the transmitter (CR5 bit 3 = 1). TxD remains in the high (marking) state. When the first character is written to the data buffer, it is transferred to the shift register and the Transmitter Buffer Becoming Empty flag is set. A parity bit, if enabled, and the specified number of stop bits (1, 1½ or 2) are appended to the character. The character plus the start bit are shifted out serially through a one-bit delay. After the character has been completely sent, the next character is loaded into the shift register and the process continues. When no more characters are available, TxD remains high and the All Async

Characters Sent flag (SR1 bit 0) is set until the next character is loaded. The transmitter may be disabled at any time (CR5 bit 3 = 0); however, transmission of the character currently being sent, if any, is completed. Disabling the transmitter does not reset the Transmitter Buffer Becoming Empty flag or any resultant interrupts or DMA requests. You can clear this flag either by writing a character to the data buffer for later transmission or by issuing a Reset Transmitter Interrupt/DMA Pending Command.

The modem control output RTS (Request To Send) may be set or reset at any time with CR5 bit 1. RTS immediately goes to the active state (low) when this bit is set. When reset, RTS does not go high until the shift register and the data buffer are empty.

The function of the modem control input, CTS (Clear To Send), depends upon the Auto Enables Control (CR3 bit 5). When Auto Enables is reset, any transition of CTS sets the External/Status Change flag but has no affect upon transmission. When Auto Enables is set, character transmission cannot begin until CTS goes low. If CTS goes high, any character currently being transmitted is completed and the transmitter is then disabled until CTS again goes low. The CTS flag, SR0 bit 5, reflects the inverted state of the external CTS pins, that is, CTS flag = 1 when CTS = low.

G-4.1.2 COP Synchronous Modes

The MPSC² gives you three distinct COP operating modes: monosync (8-bit sync character), bisync (16-bit sync character), and external sync (the transmitter operates in the same manner as Monosync). When bisync mode is selected, you should program the eight least significant bits (first byte) of the sync character into CR6 and the eight most significant bits (second byte) into CR7. For monosync and external sync modes you should program CR6 with the 8-bit sync character.

During operation in COP modes, the MPSC² transmitter may be in any one of the following phases:

Disabled Phase:	Transmitter Enable is off (CR5, D3=0) or CTS is low when the auto enables function is used;
Idle Phase:	Sync characters are being sent;
Data Phase:	Data from the processor is being transmitted;
CRC Phase:	(If CRC is used) when the CRC check characters are being transmitted.

After selecting the desired protocol and initializing parameters, the transmitter enters and remains in the Disabled Phase, with TxD high until the Transmitter Enable bit is set. Once this is done the transmitter enters the Idle Phase, transmits the first sync character and continues to send sync characters until a character is written into the transmit buffer. When the first data character is loaded into the data buffer and the current sync character has been sent, the trasnmitter enters Data Phase and sends data characters while setting the Transmitter Buffer Becoming Empty flag each time it is ready for the next character.

During the Data Phase, the transmitter may run out of data to send for one of two reasons: (1) The processor is busy and is not able to provide the next data characters within a message, or (2) the data portion of the message is complete and it is time to enter the CRC Phase (or the Idle Phase if CRC is not used). The MPSC² automatically handles both of these conditions through a mechanism called the Idle/CRC Latch, the state of which may be read from SR0 D_6.

When the transmitter is initialized the Idle/CRC Latch is set, indicating that the transmitter will enter the Idle Phase and begin sending sync characters when there is no data to send. Entering this phase also sets the Transmitter Buffer Becoming Empty flag (if not already set) to indicate with SRO $D_6 = 1$, that the Idle Phase has been entered.

However, if you reset the Idle/CRC Latch with a Reset Idle/CRC Latch command to CRO, a lack of data causes the MPSC² to enter the CRC Phase and begin sending the 16-bit CRC character calculated up to that point. Entering the CRC Phase sets the Idle/CRC Latch which, in turn, sets the External/Status Change flag indicating that the MPSC² is sending CRC. After you reset the flag, you may send the next data character to the transmitter and it will be sent immediately following the CRC, or you may do nothing. In either case, the Idle/CRC Latch is now set again so the transmitter enters the Idle Phase when no further data is available.

You can disable the transmitter during any phase of operation. If the transmitter is disabled during the Idle or Data Phases the MPSC² finishes sending the current character and goes to the Disabled Phase (TxD high). If disabled during the CRC Phase, a 16-bit CRC is sent; however, the remainder of the CRC is supplanted by sync with bit positions matching.

The CRC Generator may be programmed to either of two polynomials, CRC-16 ($x^{16} + x^{15} + x^2 + 1$) or CRC-CCITT ($x^{16} + x^{12} + x^5 + 1$). The CRC Generator may be reset to 0 at any time by issuing a Reset CRC Generator Command to CR0. Since it is sometimes necessary to exclude certain characters from the CRC calculation, the MPSC² features a CRC enable/disable control (CR5 D_0) that may be changed just prior to loading a character into the transmitter buffer to include or exclude that and subsequent characters in the CRC calculation.

G-4.1.3 SDLC (/HDLC BOP Synchronous) Mode

In SDLC mode, the MPSC² transmitter operates similarly to monosync transmission with the following exceptions:

WR6 is not used for the transmitter sync character. SDLC flags (sync) are generated internally.

Data and CRC are passed through zero insertion logic before transmission. This logic inserts a 0 bit after transmitting five contiguous ones to distinguish information from framing flags.

A special Send SDLC Abort Command is available in CR0. Issuing this command causes at least 8 but less than 14 ones to be

transmitted, destroying any data in the transmitter shift register and buffer. After sending the abort, the transmitter enters Idle Phase.

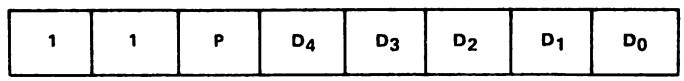
Resetting the CRC generator initializes it to all ones rather than zeroes and the result bits are inverted before transmission.

G-4.2 RECEIVER

The MPSC² receiver reverses the process performed by the transmitter. It converts the serial data stream of the various protocols back to parallel data for the processor. The major components of the receiver are shown in Figure G-4.4. Control and status registers pertinent to the operation of the receiver are summarized in Table G-4.2.

The primary data path through the receiver begins at the receiver data input RxD. Data passes through a two-bit time delay and into the receiver shift register (the sync data path is described later). The point of entry into the shift register and hence the number of bits per character is determined by the mode of operation and the Bits/Character field of CR3 (D_6-D_7). You can change this field at any time provided that the character that is currently being assembled has not yet reached the new number of bits/character. If the number of bits/character specified is less than eight, the character appears right-justified in the data buffer (with the parity bit, if parity is enabled) and the left side is filled with ones (see Figure G-4.3).

Figure G-4.3 Data Format Example for Less Than 8 Bits/Character



5 BITS/CHARACTER; PARITY ENABLED

Figure G-4.4 Block Diagram MPSC² Receiver

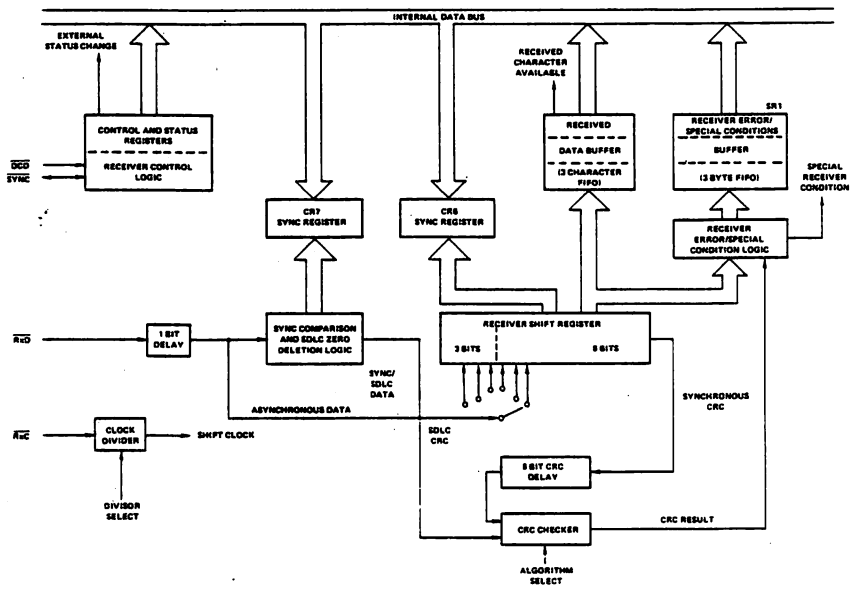


Table G-4.2 Receiver Control and Status Registers

CONTROL REGISTER	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	CRC CONTROL		COMMAND			REGISTER POINTER		
1				Receiver Interrupt Control				Ext/Status Interrupt Enable
3	Bits/Char		Auto Enables	Enter Sync Hunt Phase	Receiver CRC Enable	SDLC Address Search mode	Sync Char Load Inhibit	Receiver Enables
4	Clock Mode		Sync Format Select		Sync/Async Mode Select		Parity Control	
5						CRC Type		
6	SYNC 1							
7	SYNC 2							

STATUS REGISTER	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	Break/ Abort			Sync/Hunt Mode	DCD			Received Character Available
1	SDLC End of Frame	CRC/ Framing Error	Receiver Overrun Error	Parity Error	SDLC I-Field Residue Code			

Once the character has been assembled in the shift register, it is passed to a three-character First In-First Out buffer (FIFO) and the Received Character Available flag (and SR0 D_0) is set to inform the processor that a character is available. The three-character buffer allows the processor up to four character times to service the receiver without losing data. This feature enhances data reliability at high speeds while relaxing software timing requirements. The Received Character Available flag is reset when all characters in the buffer have been read, i.e., the buffer is empty.

As each character is transferred to the buffer, it is checked for errors or special conditions and that information is placed in a parallel FIFO error buffer so that the status associated with each character can be read with that character through status register 1. Reading a character from the data buffer moves the next character and its status to the top of the FIFO. You should read the status first, if it is of interest, and then the data.

The rate at which data is shifted into the receiver is controlled by the receiver clock input (RxC) and the clock mode field (CR4 D_6-D_7). This field also controls the transmitter clock mode. In any of the synchronous modes, you must select the 1x clock mode. In asynchronous mode you may select a divisor such that clock rate (RxC) equals 1x, 16x, 32x, or 64x the actual data rate. However, if you select the 1x mode, the clock must be externally synchronized with the data (see Section G-4.1.3). RxD is always sampled on the rising edge of RxC.

The data carrier detect (DCD) input works the same way as CTS except that it enables the receiver when auto enables is set.

G-4.2.1 Asynchronous Mode

After initializing and enabling the MPSC² Receiver, the receiver logic begins sampling the RxD input for a high-to-low (marking-to-spacing) transition on each rising edge of RxC. When the transition is found, the receiver waits ½ bit time, (for example, eight clock periods if the clock mode is 16x) and samples again to ensure that RxD is still low, improving the MPSC²'s noise immunity. If RxD is still low, the MPSC² assumes this is the middle of the start bit and one bit time later begins to sample RxD to assemble the required number of data and parity (if enabled) bits.

Once the character is assembled, the MPSC² waits one more bit time and again samples RxD. If RxD is not high, the stop bit is missing and a Framing Error is indicated when the character is passed to the data buffer. If a Framing Error has occurred, the MPSC² receiver waits ½ bit time before beginning to sample again to avoid interpreting the Framing Error as a new start bit.

Note that in the 1x Clock mode, the receiver simply waits one clock period after the first high-to-low transition is detected and then begins assembling the character. It is for this reason that data and clock must be synchronized in this mode.

The Break/Abort bit, D_7 of SR0 is set when a null character plus Framing Error is detected (i.e. RxD is low for more than one full character time). Break detection also sets the External/Status Change

flag. When RxD returns high and the break has ended, D_7 is reset to 0 and the External Status Change flag is once again set. After the break, a single null character is present in the data buffer. It should be read and discarded.

The following errors may occur during operation and are flagged in status register 1.

Framing Error	See above discussion.
Parity Error	If parity is enabled and a parity error occurs, the Parity Error bit D_4 is set. Once a Parity Error has occurred, the Parity Error bit remains set for subsequent characters until reset by an Error Reset command to CR0. You need only check the end of a message or block to determine if a parity error occurred.
Overrun Error	If the data buffer is full with three characters and a fourth character is received, the last character in the buffer is overwritten and the Overrun Error bit D_5 is set. Like Parity Error, Overrun Error remains set until the Error Reset command is issued.

G-4.2.2 COP Synchronous Modes

The MPSC² gives you three distinct COP operating modes: (1) monosync (8-bit sync character), (2) bisync (16-bit character), and (3) external sync (the SYNC pin is used as an input to inform the MPSC² that synchronization has been achieved externally).

When monosync mode is selected, CR7 should be programmed with the 8-bit sync character to be matched by the receiver.

In bisync mode CR6 should contain the least significant bits (first byte) and CR7 should contain the most significant bits (second byte) of the 16-bit character to be matched.

In external sync mode, no sync character is required by the receiver. During operation in the COP modes, the MPSC² receiver is in one of two phases: (1) Sync Hunt Phase or (2) Data Phase. The receiver automatically enters Sync Hunt Phase when it is enabled (CR3, D_0).

In monosync mode, the incoming data stream passes through and is compared to the sync character in CR7. When a match is found, the receiver switches to Data Phase and begins to pass data to the shift register. If you determine at any time that synchronization has been lost, you may re-enter the Sync Hunt Phase by setting the Enter Hunt Phase bit (D_4) in CR3. When the Hunt Phase is entered or left, the External/Status Change flag is set. When SR0 D_4 (Sync/Hunt) = one, it indicates that the receiver is in Hunt Phase.

Operation is similar in bisync mode, however, when a match is found, CR6 is also checked against the shift register contents and the Hunt Phase is left only if the bytes match. In both monosync and bisync modes, the SYNC pin is used as an output which goes momentarily low any time a sync pattern is detected whether the receiver is in Hunt or Data Phase. See Figure G-2.3 for a detailed timing diagram.

You can inhibit the transfer of sync characters to the data register by setting the Sync Char Load Inhibit bit (CR3, D_1). Since the CRC calculation on sync is not inhibited by this bit, you should use it only to strip leading sync characters from a message if you are using CRC Block Check.

Because of the 8-bit delay between the shift register and the CRC checker, CRC status (SR1, D_6) is not valid immediately after the CRC character is received. CRC status is valid 16 bit times after the last CRC character is transferred to the receive buffer, or 20 bit times after the last CRC bit is shifted in at RxD.

G-4.2.3 SDLC (/HDLC BOP Synchronous) Mode

The MPSC² provides you with high-level processing capability for handling bit-oriented protocols. When you select SDLC Mode, CR7 must be programmed with the SDLC Flag character 01111110.

When operating in SDLC mode, the receiver can be in one of three phases: Hunt Phase, Address Search Phase, or Data Phase.

The receiver automatically enters Hunt Phase when first enabled. The incoming data stream passes through the one-bit delay and enters the Sync Comparison/Zero Deletion logic where the following three operations are performed.

First, whenever a 0 bit follows five consecutive ones, that 0 is deleted from the data stream. Second, if six consecutive ones are received, a Flag Character Received indication is given internally. Third, if eight or more ones are received, an abort is indicated and the External/Status Change Flag is set. Flags and aborts are not transferred to the receiver shift register.

Once a flag is detected, the receiver leaves Hunt Phase (setting the External/Status Change Flag) and, if Address Search Mode (CR3-D_2) is enabled, it enters Address Search Phase. Once this phase is entered, the MPSC² receiver compares the first 8-bit non-flag character with the contents of control register 6. If the two values match, or the received character is the global address 11111111, the receiver immediately enters Data Phase and character assembly begins with this character. If no match is found and the value is not the global address, the receiver remains in Address Search Phase and no data characters are assembled until a flag followed by the correct address is encountered. If Address search Mode is not enabled, Data Phase is entered immediately and character assembly begins with the first non-flag character. Since all messages are framed with flag characters, you can skip an incoming message at any time simply by setting the Enter Hunt Phase bit (D_4) in CR3.

Once in Data Phase, characters are assembled according to the number of bits or characters specified until the next End of Frame flag is encountered. The receiver then sets the Special Receive Condition flag and transfers the character currently being assembled to the receiver buffer regardless of the number of bits actually assembled. A special residue code placed in the status buffer (SR1) uses the number of bits assembled to indicate the boundary between the data and CRC characters (see Section G-5.1 for a more detailed